88EM8040/88EM8041

Power Factor Correction Controller for Flyback Topology

Datasheet

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PRODUCT OVERVIEW

The Marvell® 88EM8040/88EM8041 device is a high performance Power Factor Correction (PFC) Controller for flyback applications. Both devices work at fixed frequencies, 88EM8040 at 60kHz while 88EM8041 at 120kHz. It can be used in a wide variety of universal input PFC flyback converters with an output power range of up to 150W without using any external driver.

Marvell advanced mixed signal technology ensures the lowest Total Harmonic Distortion (THD) in the industry. The IC operates under average Continuous Conduction Mode (CCM).

The 88EM8040/88EM8041 PFC controller improves the steady state and transient performance through Marvell's innovative Digital Signal Processing (DSP) solution. The proprietary adaptive over-current protection has the ability to ensure almost constant power constraint and provides safety provisions including open loop and over voltage protection protocols.

The internal voltage loop compensation and current loop control guarantees system stability and thus reduces the external component count and costs.

The 8-pin SOIC package further facilitates the application design process, saving board space. The resultant simple system design and minimum cost makes 88EM8040/88EM8041 the ideal choice for any flyback application with PFC.

General Features

- **Patented DSP control with adaptive loop coefficient**
- **Continuous Conduction Mode (CCM) operation**
- **Average current mode control**
- **Adaptive control loop achieves high power factor for a wide range of voltage and load conditions**
- **Adaptive over current protection for universal voltage**
- Fixed frequency of operation
- High power factor and low harmonic distortion for a wide range of load conditions
- Up to 2A driver capability
- Minimal external components required
- Under voltage lockout (UVLO)
- Over voltage protection (OVP)
- Thermal shutdown
- Input line frequency range from 45Hz to 65Hz

Applications

- Universal input PFC flyback converters
- AC/DC adaptors and battery charger

Figure 1: PFC Flyback Circuit Diagram

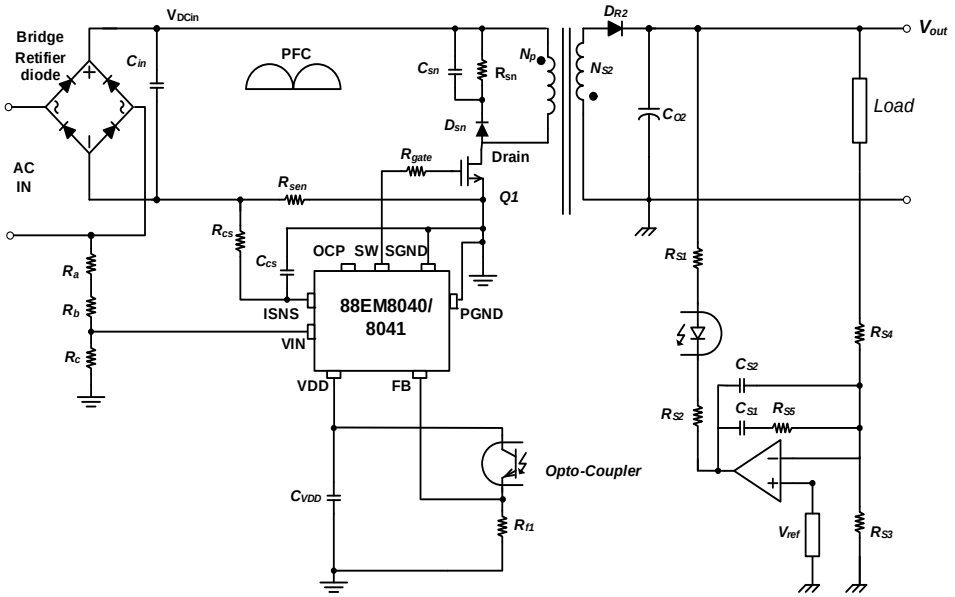

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Table of Contents

List of Figures

List of Tables

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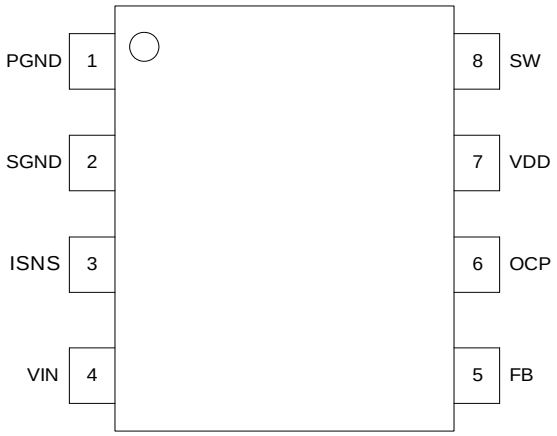
1 Signal Description

1.1 Pin Configurations

Figure 2: SOIC-8 Pin Diagram (Top View)



1.2 Pin Descriptions

Table 1: Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	PGND	Ground	Power Ground
2	SGND	Ground	Signal Ground
3	ISNS	Input	Current Sense
4	VIN	Input	Voltage Input
5	FB	Input	Feedback
6	OCP	Input	Over Voltage Current Protection
7	VDD	Supply	IC Supply Voltage
8	SW	Output	Switch

Table 2: Pin Descriptions

Pin #	Pin Name	Pin Function
1	PGND	**Power Ground** Connected to the source of the primary MOSFET. The PCB trace from the power ground to the source of the primary MOSFET must be kept as short as possible. To avoid any switching noise interruption on signal processing, PGND and SGND remain seperate inside the IC.
2	SGND	**Signal Ground** Must be connected to the power ground with the Kelvin sensing connection, so that SGND has dedicated trace and connections and provides noiseless environment for the signal processing.
3	ISNS	**Current Sense** Sense resistor varies from 0.15Ω at 120W rated load to 0.44Ω for 40W rated load. Used for current shaping and for over current protection.
4	VIN	**Voltage Input** • Connects to resistive divider at input AC line “phase” to GND. Voltage applied is a half rectified sine wave scaled down by the input resistive divider. • Voltage input pin is a high impedance input pin. An impedance of 2M (typical) is recommended to be designed from the input AC “phase” to GND in order to reduce the standby power. Higher impedance is preferred with the right PCB design on this pin signal. • Voltage is compared with a threshold reference (V_{VIN_BR}) to detect the zero-cross location of the input sine wave and synthesize (regenerate) the input sine wave. This sine wave is used to generate the current reference. • Brown-out protection[1] function is also provided by this pin. A resistor devider with a 100:1 ratio from the highside resistor to the lowside resistor is corresponding to the “brown-out protection” input voltage as 50V (RMS). Increasing that raio will increase the “brown-out voltage”. Please refer to footnote[1] for further explaination.
5	FB	**Feedback** It is connected to the emitter of the transistor on the secondary side of the opto coupler (referred to within the Appication Information section). The output voltage is scaled to 2.5V with 100% rated value. Transition from soft start to normal regulation at 87.5% rated V_{FB}. Over voltage shutdown SW gate signal at 107% rated V_{FB} and recover once below V_{FB_OVP}. There is another threshold ($V_{FB\_OVP\_LATCH}$) as 3.77V on the FB pin. When FB Voltage reaches $V_{FB\_OVP\_LATCH}$, SW signal is shutdown and latched until another VDD power on reset.
6	OCP	**Over Current Protection** Used to turn off the MOSFET when it is pulled as logic low
7	VDD	**IC Supply Voltage** Nominal voltage is typical 12V and the Under Voltage Lock Out (UVLO) for $V_{DD} < V_{DD\_UVLO}$ (Table 5). Start voltage of IC is V_{DD_On} (Table 5) and maximum voltage is 16V (Table 5). It should be clamped by a zener for protection in the system design.
8	SW	**Switch** PWM gate signal for the switch. Connects to the gate of external MOSFET. It is the DSP core output for ON/OFF time buffered through the internal adaptive driver.

1. Brown-out voltage is determined by R_a, R_b and R_c as shown in Figure 1. Please refer to page 29 for a further understanding.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings[1]

NOTE: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Units
V_{DD}	Power Supply (Voltage to PGND=SGND)	-0.3	18	V
V_{Isns}	Voltage at ISNS pin	-0.5	3	V
V_{OCP}	Voltage at OCP pin	-0.3	5.5	V
V_{VIN}	Voltage at VIN pin	-0.3	5.5	V
V_{FB}	Voltage at FB pin	-0.3	5.5	V
I_{SW}	Driver Current (Instantaneous Peak)		2	A
θ_{JA}	Thermal Resistance SOIC-8		156.5	°C/W
	Thermal Resistance DIP-8		89.5	°C/W
T_A	Operating Ambient Temperature Range[2]	-40	85	°C
T_J	Maximum Junction Temperature		125	°C
T_{STOR}	Storage Temperature Range	-65	150	°C
V_{ESD}	ESD Rating[3]		2	kV

1. Exceeding the absolute maximum rating may damage the device.
2. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5kΩ in series with 100pF.

2.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
T_A	Operating Ambient Temperature[2]	-40		85	°C
T_J	Junction Temperature	-20		125	°C

1. This device is not guaranteed to function outside the specified operating temperature range.
2. Over the –40°C to 80°C operating temperature ranges are assured by design, characterization, and correlation with statistical process controls.

2.3 Electrical Characteristics

Table 5: Electrical Characteristics

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply						
V_{DD}	Supply Voltage		7.0	12	16	V
V_{DD_ON}	V_{DD} Power On Threshold			11.9		V
V_{DD_UVLO}	V_{DD} Power Off Threshold (UVLO)	After V_{DD} is powered up and running		7.0		V
$V_{DD\_UVLO\_HYS}$	V_{DD_UVLO} Hysteresis		4.8		5	V
I_{DD_QST}	V_{DD} Quiescent Current[1]	V_{DD} = 12V			95	µA
I_{DD_OP}	V_{DD} Operating Current	V_{DD} = 12V; C_{Gate} = 1nF F_{SW} = 118kHz V_{IN}=0		5.2		mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown		150			°C
T_{SD_HYS}	Hysteresis for Thermal Shutdown		25			°C
Adaptive Output Gate Driver						
V_{G_HI}	Minimum Gate High Voltage[2]	V_{DD} = 12V C_{Gate} = 1nF Sourcing 500mA	10.0			V
V_{G_LO}	Maximum Gate Low Voltage[3]	V_{DD} = 12V C_{Gate} = 1nF Sinking 500mA			2.0	V
R_{DSON}	Gate Drive Resistance	Sourcing 75mA T=25°C		2.4		Ω
	Gate Drive Resistance	Sinking 20mA T=25°C		2.0		Ω
I_{SW_PK}	Driver Peak Current	C_{Gate} = 10 nF V_{DD} = 12 V	2.0			A
t_R	Rise Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		125		ns
t_F	Fall Time	C_{Gate} = 1 nF		35		ns
		C_{Gate} = 10 nF		145		ns
D_{MAX}	Maximum Duty Cycle				97	%

Table 5: Electrical Characteristics (Continued)

NOTE: A 12V supply voltage is applied and the ambient temperature (T_A) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
D_{MIN}	Minimum Duty Cycle		3.0			%
Feedback/Overvoltage						
V_{FB_REG}	Normal Regulation Reference	IC powered on		2.55		V
V_{FB_OVP}	Over Voltage Protection Threshold	At 107% of V_{FB_REG}.		2.71		V
$V_{FB\_OVP\_HYS}$	Over Voltage Protection Hysteresis				0.108	V
$V_{FB\_OVP\_LATCH}$	Over Voltage Protection Latch			3.77		V
Current Sensing and Current Protection[4]						
V_{IOVER_TH1}	Over Current Threshold Zone 1[5]	Peak value of half-sine voltage at V_{IN}: $1.26<V_{IN}<1.89V_{pk}$[6]		397		mV
V_{IOVER_TH2}	Over Current Threshold Zone 2[5]	Peak value of half-sine voltage at V_{IN}: $1.89<V_{IN}<2.59V_{pk}$[7]		329		mV
V_{IOVER_TH3}	Over Current Threshold Zone 3[5]	Peak value of half-sine voltage at V_{IN}: $2.59< V_{IN}<3.43V_{pk}$[8]		269		mV
V_{IOVER_TH4}	Over Current Threshold Zone 4[5]	Peak value of half-sine voltage at V_{IN}: $3.43<V_{IN}<3.85V_{pk}$[9]		202		mV
$V_{IOVER\_CYC\_ON}$	Cycle by cycle current protection logic input (OCP pin) threshold for SW on[10]			1.68		V
$V_{IOVER\_CYC\_OFF}$	Cycle by cycle current protection logic input (OCP pin) threshold for SW off[11]			1		V
88EM8040 Switching Frequency Oscillator						
F_{SW}	Frequency (Average Mode)					kHz
88EM8041 Switching Frequency Oscillator						
F_{SW}	Frequency			118		kHz

1. Quiescent Current: V_{DD} power supply current before V_{DD} first time reaches $V_{DD\ On}$.
2. Considering the voltage drop on the internal driver MOSFET during current sourcing.
3. Considering the voltage drop on the internal driver MOSFET during current sinking.

4. To achieve almost constant power limit for the universal input range, current protection self-adjusts thresholds in four zones of input voltage levels. A margin of 50% compared to the rated current is considered for the threshold current values.
5. Threshold of negative voltage drop across R_{sns} due to instantaneous current
6. With input divider ratio of 1/100, these values are equivalent to 90 V_{rms}<V_{line}<135 V_{rms}.
7. With input divider ratio of 1/100, these values are equivalent to 135 V_{rms}<V_{line}<185 V_{rms}.
8. With input divider ratio of 1/100, these values are equivalent to 185 V_{rms}<V_{line}<245 V_{rms}.
9. With input divider ratio of 1/100, these values are equivalent to 245 V_{rms}<V_{line}<275 V_{rms}.
10. When OCP pin is above $V_{IOVER\ CYC\ ON}$ as 1.68V, then SW is controlled by the PWM block for on and off.
11. When OCP pin is below $V_{IOVER\_CYC\_OFF}$ as 1V, then SW is turned off and released at the next switching cycle if OCP pin is above $V_{IOVER\_CYC\_ON}$

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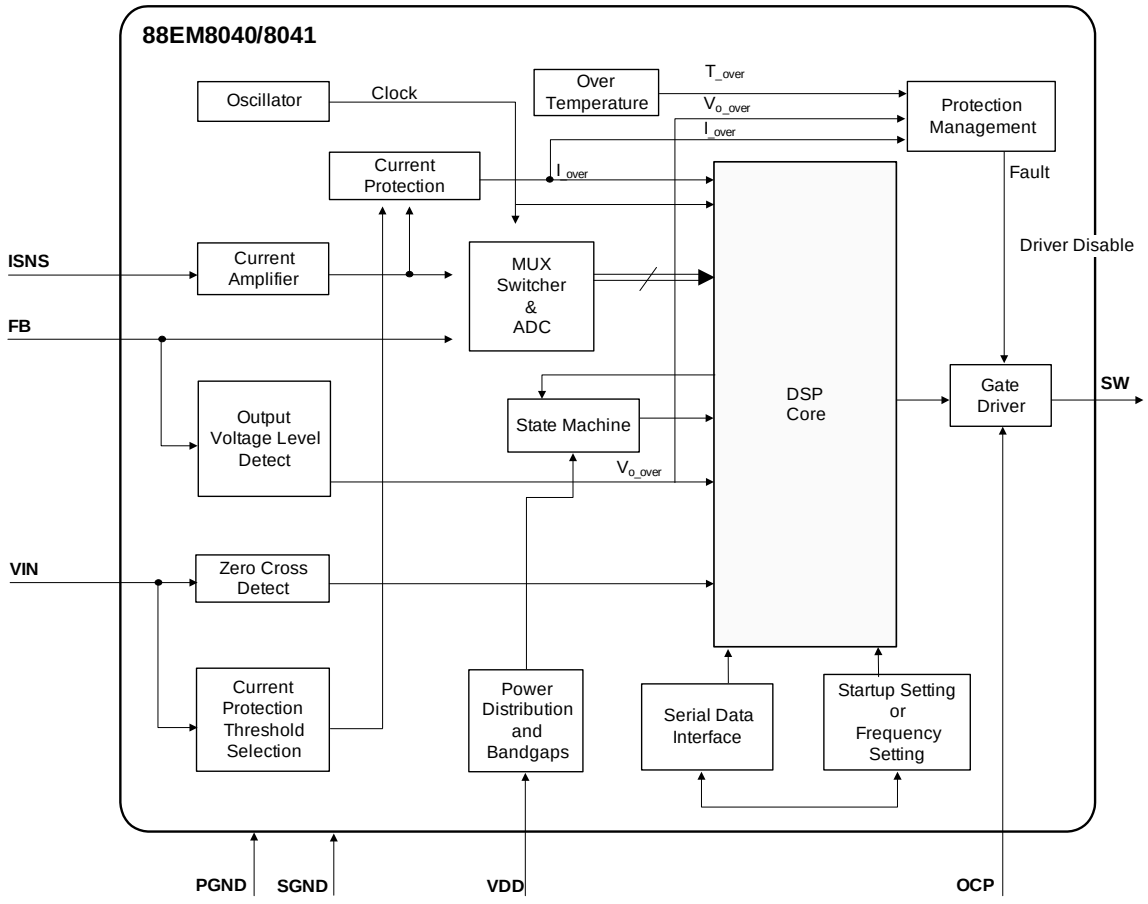
3 Functional Description

3.1 Overview

The 88EM8040/88EM8041 is a high performance, low-cost with minimum component count Power Factor Correction (PFC) Controller. The device is used for controlling Universal input flyback converters in systems or standalone products. The high performance of 88EM8040/88EM8041 is accompanied with its small size and simplicity of application. Figure 3 shows the top level block diagram.

Figure 3: Top Level Block Diagram



Note

- I_{over}, V_{o_over}, and T_{over} are the over current, over voltage, and over temperature signals respectively.

3.2 Signal Process and Functions

The 88EM8040/88EM8041 boost power board includes three inputs:

- Resistive divider signal from AC line voltage
- Feedback from the output DC bus
- Voltage across the current sense resistor

The input phase voltage to ground (half rectified sine wave) scaled down by the input resistive divider is applied to pin V_{IN}. This signal used for estimation of the AC line voltage and regeneration of the AC sine wave. It is also used for voltage level detection that produces adaptive multiple thresholds for the over current limit and guarantees a constant power limit from the AC source.

Signal from the DC bus voltage through the muxed 12-bit Analog-to-Digital Converter (ADC) provides the feedback data for the voltage PI control loop.

HF switching current pulse signal is retrieved from the voltage drop across the current sense resistor that is negative to GND. This signal after HF noise filter and fixed gain amplification, is transferred through the muxed 12-bit ADC to the digital current loop and the current error amplifier. The reference current for the current control PI loop is provided by multiplying the voltage error amplifier output and the regenerated sinusoidal line voltage information.

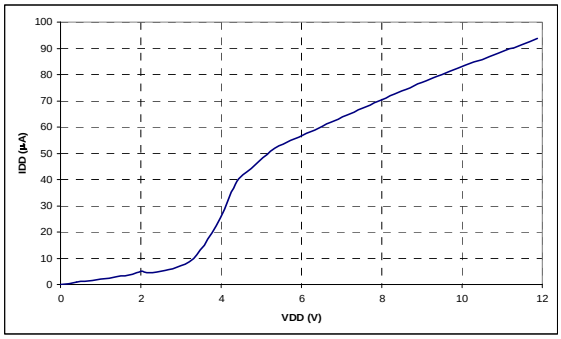
4 Functional Characteristics

The following applies unless otherwise noted: V_{IN} = 60Hz half-wave sinusoidal from 0V to the peak voltage (V_{PK}) given in the test conditions of each graph. T_A = 25°C.

All measurement readings are typical.

4.1 V_{DD} Characteristics

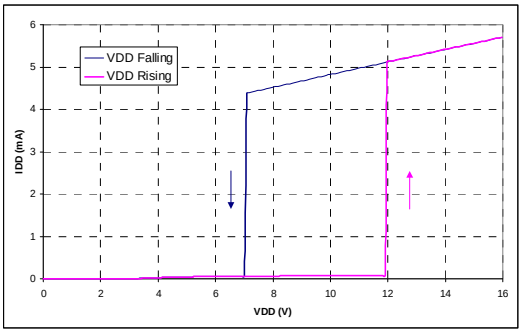
Figure 4: I_{DD} Quiescent (I_{DD_QST}) vs. V_{DD}



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- V_{FB} = 0V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

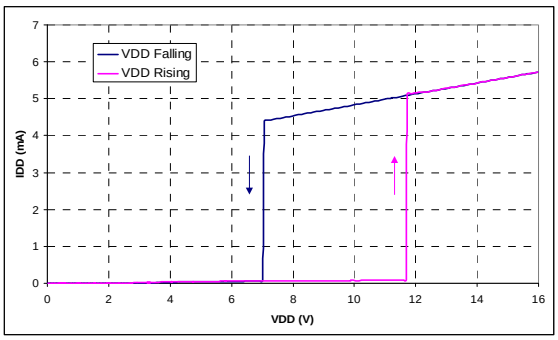
Figure 5a: I_{DD} vs. V_{DD} (V_{DD_ON})



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

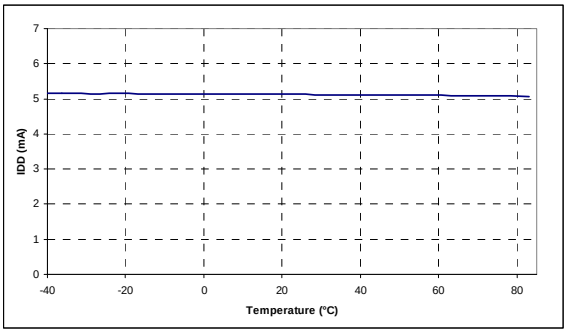
Figure 5b: I_{DD} vs. V_{DD} (V_{DD_ON})



Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

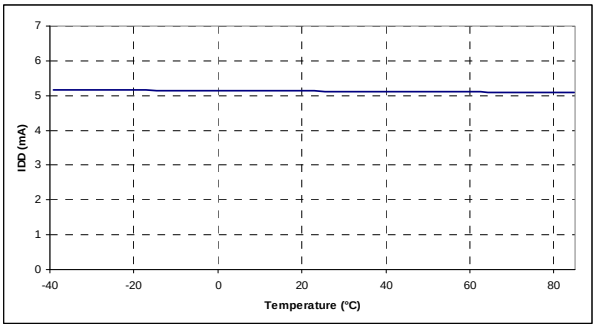
Figure 6a: I_{DD} Operation (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 0V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

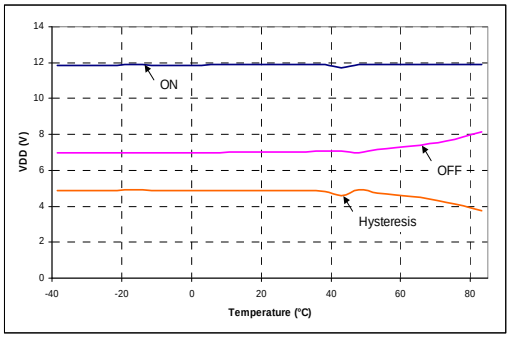
Figure 6b: I_{DD} Operation (I_{DD_OP}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- **V_{FB} = 2.4V**
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 7: V_{DD} On/Off vs. Temperature

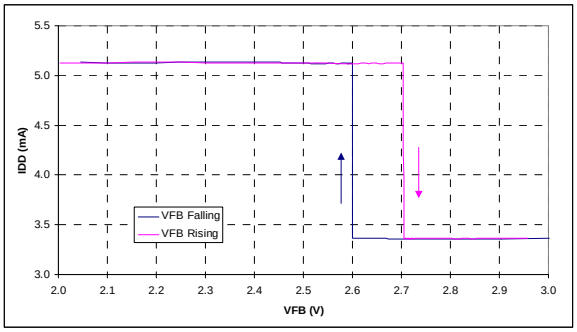


Test Conditions:

- V_{IN} = 0V
- F_{SW} = 118kHz
- F_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.2 V_{FB} Characteristics for Over Voltage Protection

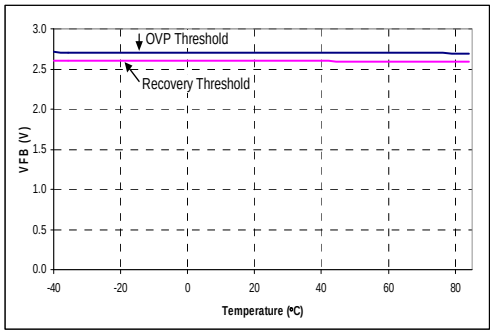
Figure 8: I_{DD} vs. V_{FB} (OVP)



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

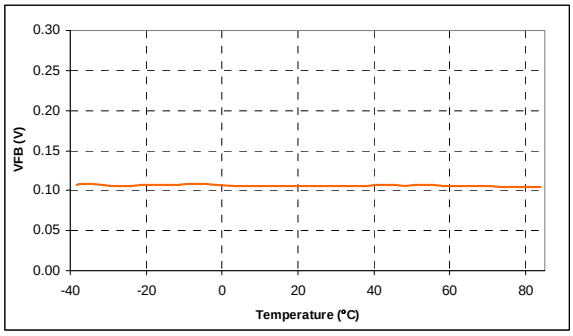
Figure 9: V_{FB_OVP} vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

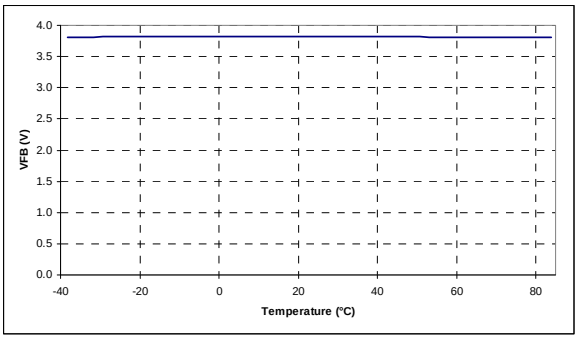
Figure 10: V_{FB_OVP} Hysteresis vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

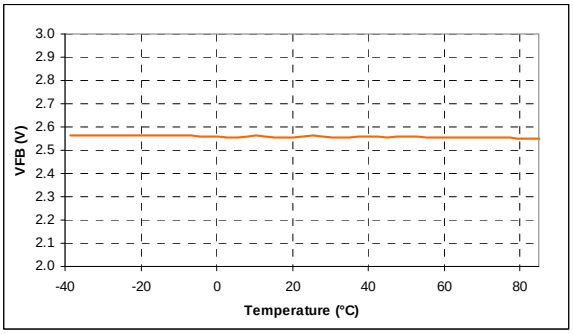
Figure 11: $V_{FB\_OVP\_LATCH}$ vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 12: Normal Regulation Reference (V_{FB_REG}) vs. Temperature

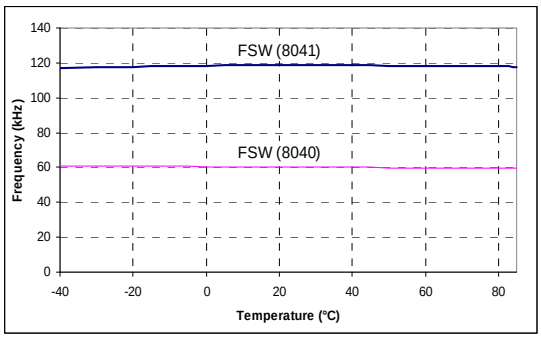


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 2V
- F_{SW} = 118kHz
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.3 Switching Frequency Characteristics

Figure 13: Switching Frequency vs. Temperature

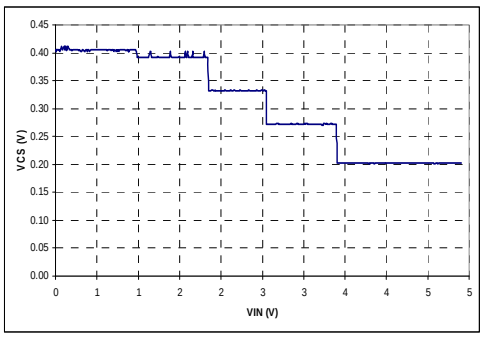


Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

4.4 Over Current Threshold Characteristics

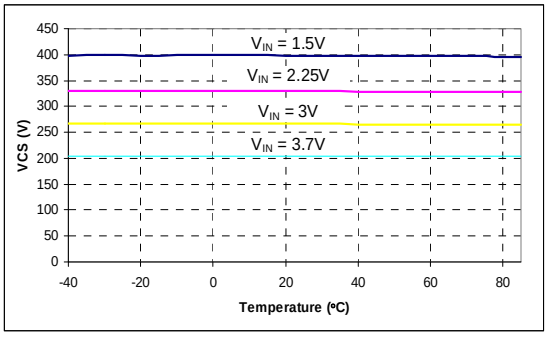
Figure 14: Over Current (V_{IOVER}) vs. Input Voltage V_{IN} Peak Value)



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

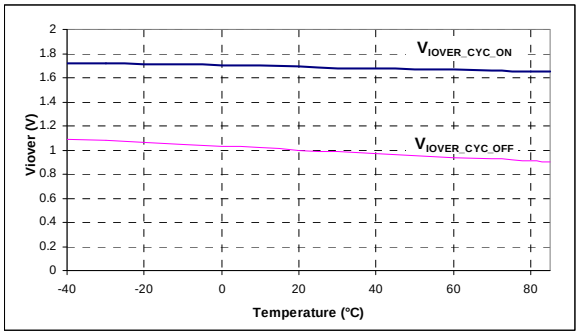
Figure 15: Over Current (V_{IOVER}) vs. Temperature



Test Conditions:

- V_{DD} = 12V
- F_{SW} = 118kHz
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

Figure 16: $V_{IOVER\_CYC\_ON/OFF}$ vs. Temperature



Test Conditions:

- V_{DD} = 12V
- V_{IN} = 0V
- V_{FB} = 2.4V
- C_{Gate} = 1nF
- V_I_{sns} = 0V

5 Design and Applications Information

The flyback (isolated buck/boost) topology is used to simplify the two stage front-end design to a single isolated Power Factor Correction (PFC) conversion stage. Compared to the two stage PFC structure, a single stage PFC is a more cost effective solution.

The 88EM8040/88EM8041 chip control algorithm uses Average Current Mode Control for power factor correction applications with low harmonic distortion and good noise immunity. The IC senses the output voltage and forces it to follow the reference voltage to produce a stable DC output voltage matching the design requirements. It also senses the primary current and forces the average signal of the primary current to follow the sinusoidal current reference, therefore achieving power factor correction. Compared to other competitors parts operating under Critical Transition Mode Control, the 88EM8040/88EM8041 has many advantages as shown in Table 6l

Table 6: Comparison Between Average Current Mode and Critical Transition Mode Control

Critical Transmition Mode Control	Average Current Mode Control
High peak current on switch	Low peak current on switch
High diode peak current at secondary side	Low diode peak current at secondary side
Variable switching frequency with lowest switching frequency at peak input voltage	Fixed switching frequency
Big transformer	Small transformer
Low efficiency	High efficiency
Low power factor / higher THD at high line low load	High power factor / lowerer THD at high line low load due to adaptive loop control
Difficult to achieve high power	Easy to achieve high power
High cost	Low cost

Marvell's innovative PFC control technology improves the performance of the isolated flyback converter used in PFC applications. The flyback PFC solution based on the 88EM8040/88EM8041 provides customers with a simple structure, low cost without sacraficing performance compared with the other industry solutions currently on the market.

The following sections provides guidelines for the application design, component selection, and board layout all in order to improve flyback single stage PFC performance. There are three analog input signals and one logic input signal listed below are required from the power train to the controller IC 88EM8040/88EM8041.

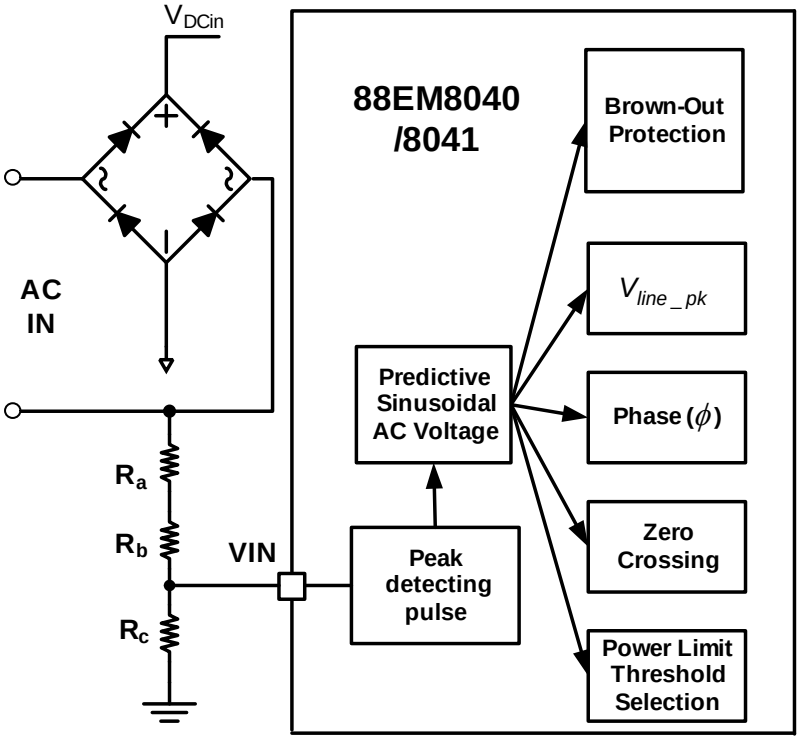
1. Input voltage signal at VIN pin is a half sinusoidal waveform. It is fed into the VIN pin through the input voltage resistor divider. This is for the line frequency zero-cross detection for PFC.
2. Output voltage signal at FB pin is the output voltage through the resistor divider plus the compensation and opto-coupler to feedback on FB pin. This is for the voltage loop regulation.
3. Current sensing signal through the sensing resistor to the ISNS pin. This is for the average current mode control to achieve a good sinusoidal current waveform and high power factor.
4. The input over current protection (OCP) signal is a logic signal instead of an analog signal. It is used to shut down the output at the SW pin when it is pulled low.

The output signal from the 88EM8040/88EM8041 is the PWM gate drive signal from the SW pin. The switching frequency on the 88EM8040 device is fixed to 60kHz while the 88EM8041 is fixed to 120kHz. Both device tolerances are shown in the electrical characteristics table.

5.1 Input Voltage Resistor Divider on VIN Pin

An accurate peak detection signal and zero-cross detection for regenerating the input sinusoidal voltage is the most important issue for a proper current shaping and total harmonic distortion (THD) improvement. If the threshold reference is too high, near the peak area, the calculation may lose accuracy because of the low slope. On the other hand, if the threshold reference is too low, there could be an error on zero-cross detection due to the possible distortions near the zero-crossing. For a universal input voltage range (85Vac~270Vac) the optimum accuracy would be achieved if the threshold level is around 30 degree of the line cycle.

Figure 17: Internal Block for Zero-cross Detection, Brown-out Protection

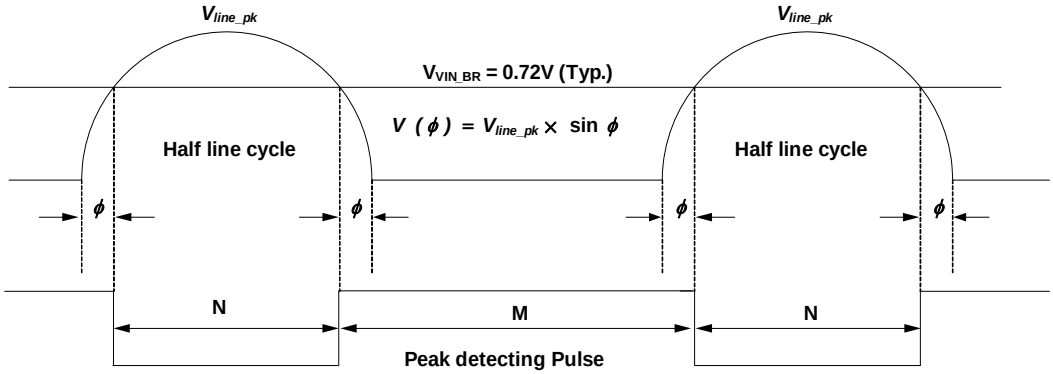


To get a proper sinusoidal AC voltage, UVLO, and peak voltage detection, we need to choose the right value for the sensing resistors: R_a, R_b, and R_c, as shown in Figure 17. If the value is too small there will be higher power loss and if the value is too big the resistor will not properly work due to the picking noise of the VIN signal. The recommended values are shown below:

$$\frac{R_a + R_b}{R_c} = \frac{100}{1} = \frac{1.8M\Omega}{18k\Omega}$$ Equation (1)

For the input voltage resistor divider, the appropriate combination based on the voltage / power rating of the resistors should also be considered.

Figure 18: Peak Detecting Signal for Predictive Sinusoidal AC Voltage



As can be seen in Figure 17, the internal peak detecting circuit generates peak detecting pulse through the inside comparator which has a threshold voltage of 0.72V (typical). Processing of this pulse in DSP core calculates the mid-point (peak point) and the zero-crossing point of the sinusoidal waveform. The phase angle of ϕ is calculated using the width of the high and low signal M&N.

$$N = (\pi - 2\phi) \quad \text{Equation (2)}$$

$$M = (\pi + 2\phi) \quad \text{Equation (3)}$$

$$\phi = (M - N)/4 \quad \text{Equation (4)}$$

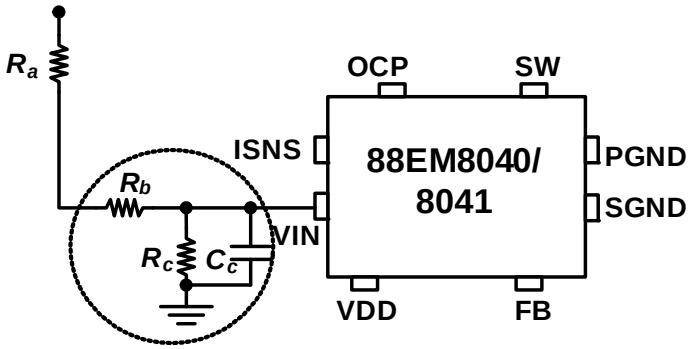
Peak value of the sinusoidal waveform is introduced by the relation:

$$V_{\text{line\_pk}} = V(\phi)/\sin(\phi) \quad \text{Equation (5)}$$

The signal that appears on the VIN pin is a half sinusoidal voltage waveform and its peak line value has to be higher than V_{VIN_BR} of 0.72V (typical) for normal operation. Whenever the V_{VIN_BR} is less than 0.72V at the peak line value, it is considered as a Brown-out condition. The IC only generates 6% duty during the brown-out condition. To adjust the brown-out protection point, the resistance value of R_a, R_b and R_c can be changed. With the recommended resistor values in Equation (1) the brown-out protection voltage is 72V peak value, which is around a 50V RMS value for the input line voltage.

The layout of R_a, R_b and R_c should be kept as close as possible to the VIN pin, as shown in Figure 19 in order to have a proper layout on the input voltage resistor divider and to avoid noise picking. It is also recommended that a 0.1nF–10nF capacitor is connected between the VIN pin and ground with the layout also close to this pin.

Figure 19: Input Voltage Resistor Divider Layout Guidelines



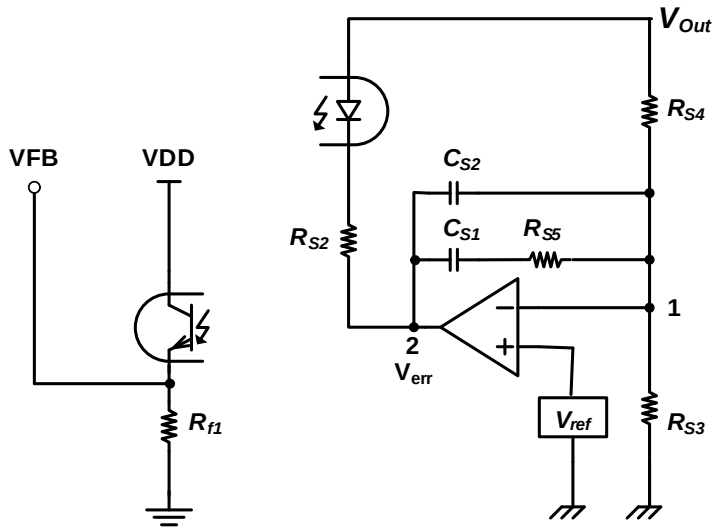
Keep layout of Rb, Rc and Cc as close as possible to Vin pin to keep high noise immunization

5.2 Isolated Voltage Loop and Output Voltage Feedback on FB Pin

The88EM8040/88EM8041 IC integrates the voltage loop into digital DSP core. This internal voltage loop has the lower corner frequency for the PFC requirement. The FB pin is the internal voltage loop feedback signal input. The voltage reference of the IC is 2.5V for the rated output voltage.

The Flyback PFC is an isolated power system, which needs the opto-coupler device transferring the output voltage amplitude signal to the FB pin. Since the CTR (Current Transfer Ratio) parameter of this opto-coupler has a big tolerance and shifts with the temperature, an additional voltage reference and compensation is required at the secondary side. This secondary voltage loop circuit can use a low voltage adjustable shunt regulator such as the TLV431 or a dual op-amp with a reference voltage such as the TSM1014 to constitute the error amplifier with compensation network. Figure 20 shows the typical voltage feedback loop circuit.

Figure 20: Secondary Compensation Network with Opt-coupler



It is well known that a single stage PFC with flyback topology is not easy to maintain enough stability while at the same time keeping a good sinusoidal current waveform and power factor under a wide input voltage and load condition. In order to achieve enough stability as the first criteria, the compensation network at the secondary should be designed properly, which will be described in the following paragraph. In order to achieve a good sinusoidal current waveform and power factor, the voltage loop regulation coefficient should also be designed properly corresponding to the different input voltages. The adaptive voltage loop coefficient is designed inside the IC to select different voltage regulation parameters. This achieves a much better power factor and sinusoidal current waveform compared to any of the single stage PFC power system on the market now. This is why there is also another voltage loop regulation designed inside of the IC while an external voltage loop compensation is designed at the secondary side of the flyback system.

5.2.1 Resistor Divider Design for Output Voltage

The design of R_{S3} and R_{S4} is based on the rated output voltage and the power loss of the resistor divider. In order to keep low power consumption on the resistor divider and good signal to noise immunity, a minimal total resistance of 20kΩ (Typical) is recommended for the pair of resistors R_{S3} and R_{S4}.

The relation among the output voltage, reference voltage and resistor divider is as;

$$V_{out} \times \frac{R_{S3}}{R_{S3} + R_{S4}} = V_{ref} \qquad \text{Equation (6)}$$

If the output voltage is designed as 20V, reference voltage is 2.5V and R_{S4} is selected as 15.4kΩ, the value R_{S3} is calculated from equation (6) as 2.21 kΩ.

5.2.2 Compensation Network Design[1]

The compensation network should be designed by selecting the value of R_{S5}, C_{S1} and C_{S2}. A typical compensation network is constructed in Figure 20. The transfer function is derived as;

$$H(s) = \frac{V_{err}(s)}{V_{OUT}(s)} = \frac{1}{R_{S4}(C_{S1} + C_{S2})} \times \frac{1 + sR_{S5}C_{S1}}{s\left(1 + s\frac{C_{s1}C_{s2}}{C_{S1} + C_{S2}}R_{S5}\right)} \qquad \text{Equation (7)}$$

Equation (7) is simplifed as;

$$H(s) = K \times \frac{(s + \omega_z)}{s(s + \omega_p)} \qquad \text{Equation (8)}$$

Where:

$$K = \frac{1}{R_{S4}C_{S2}} ; \omega_z = \frac{1}{R_{S5}C_{S1}} ; \omega_p = \frac{1}{\frac{C_{S1}C_{S2}}{C_{S1} + C_{S2}}R_{S5}} \qquad \text{Equation (9)}$$

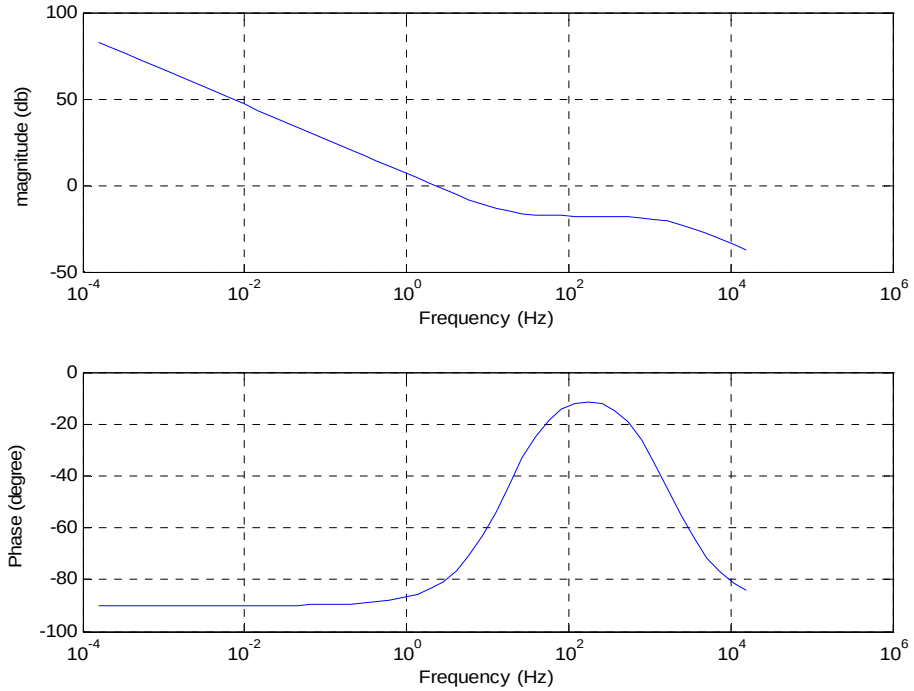
The criteria to design the network in Figure 20 is to provide enough DC gain and attenuate the double line frequency ripple by properly selecting the right zero and pole parameters. In order to meet these criteria, zero ω_z should be placed below the double line frequency (100/120Hz) and pole

1. Please refer to the 88EM8041 90W application note for a detailed derivation of open-loop transfer function for the overall flyback circuit.

ω_p should be placed above the double line frequency. The magnitude of the gain around the double line frequency should below the unity gain, which is 0db axis in the bode plot, in order to attenuate the double line frequency ripple.

The following is a design example of this network: R_{S4}=15.4kΩ, R_{S5}=2kΩ, C_{S1}=4.7μF and C_{S2}=47nF. This produces a zero and pole as: ω_z = 16.94Hz, ω_p = 1.71kHz. The bode plot is shown in Figure 21. The magnitude of the gain at 100Hz to 120Hz is about -18dB, therefore the double line frequency ripple is attenuated. The parameters are designed to maintain the stability for the single stage PFC system.

Figure 21: Bode Plot of Compensation Network at Secondary Side



In order to decrease the time for the transconductance error amplifier at the secondary to quit the saturation process and reduce the output voltage overshoot at startup, a Zener diode is required. The zener diode is connected between the error amplifier output terminal to ground. This reduces the overshoot and improves the startup performance, because the zener provides a bias current before the transconductance error amplifier sinks current. Because of the tolerance of the opto-coupler CTR, the output voltage of the error amplifier under a steady state should not become too low so as to keep the sufficient output regulation capability.

In the 20V/90W reference design, a 6.8V Zener is selected and output of the error amplifier is set as about 5 to 6 volts under steady state. The output voltage of the transconductance error amplifier is around one third of the rated output voltage under steady state.

5.2.3 R_{S2} and R_{f1} Design

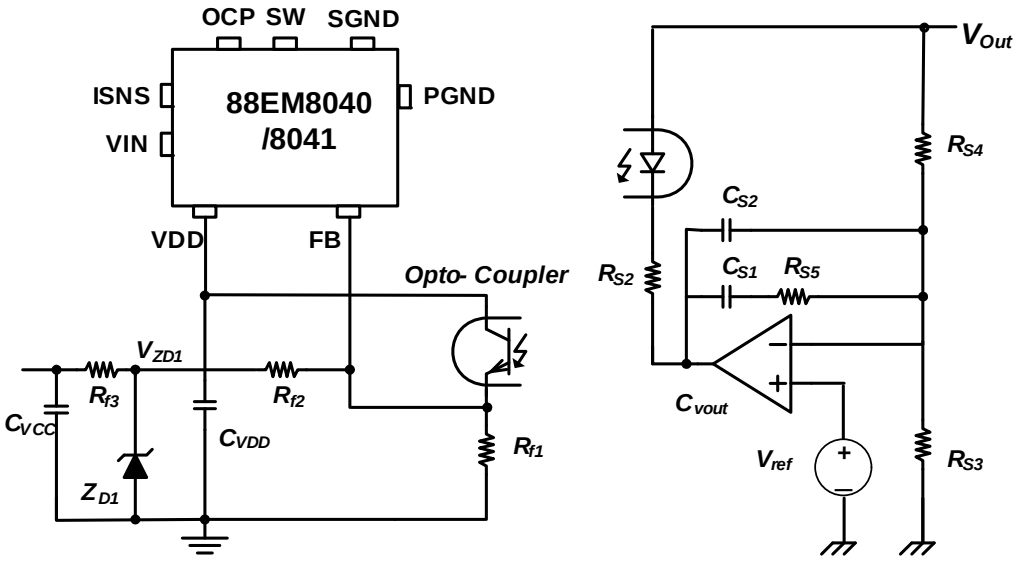
The R_{S2} and R_{f1} design is mainly based on the opto-couplers current transfer ratio(CTR) Which should be around 100% to 200%. R_{S2} is designed to produce around 1mA current at the LED side of the opto-coupler. R_{f1} is designed to produce 2.5V feedback voltage to close the loop under a stead state. If R_{f1} is designed at 1.24kΩ, the current at transistor side of the opto-coupler should be designed at 2mA (typical). This should have enough signal to noise ratio in the practical design. The feedback resistor (R_{f1}) should be kept close to the opto-coupler to avoid noise in the layout.

The output of PFC Flyback has double line frequency ripple voltage. At the steady state operation condition, the FB pin voltage transferred from secondary side also has this double line frequency ripple voltage. The ripple voltage amplitude on the FB pin is determined by the output voltage ripple amplitude and the gain from the output voltage to the FB pin (referred in the previous section Section 5.2.2, Compensation Network Design, on page 31). It is noticed that there is an attenuated ripple appearing at the output of the amplifier with the minus phase shift from the output voltage ripple. Therefore, the ratio of ripple voltage amplitude over the DC voltage value of FB pin is bigger than the ratio of output ripple over DC output voltage. If the output ripple voltage is too big in certain applications, the FB pin voltage peak value might trigger the internal FB OVP threshold, which is about 7% on the top of the reference value. This will heavily distort the input current waveform and disturb the stability of the system. In order to solve this issue, it is recommended to use a constant offset voltage circuit, as show in Figure 22. This circuit consists of a diode (Z_{D1}), and two resistors (R_{f2} and R_{f3}). This will provide a bias current from the bias winding so as to produce a bias voltage on the FB pin. Therefore, the ripple voltage amplitude of the FB pin is decreased below the FB OVP threshold. In the 90W reference design, the winding bias voltage provides 1mA (typical) offset current to the FB pin and the ripple voltage amplitude on the FB pin can decrease to be around half of that with this bias circuit. R_{f2} can be calculated by equation (10), in which V_{FB} is 2.5V reference voltage.

If the cathode voltage V_{ZD1} is 9.1V, R_{f2} is calculated as 6.8kΩ·

$$\frac{V_{ZD1} - V_{FB}}{R_{f2}} = 1mA \qquad \text{Equation (10)}$$

Figure 22: Bias Current for Offset Voltage on FB Pin

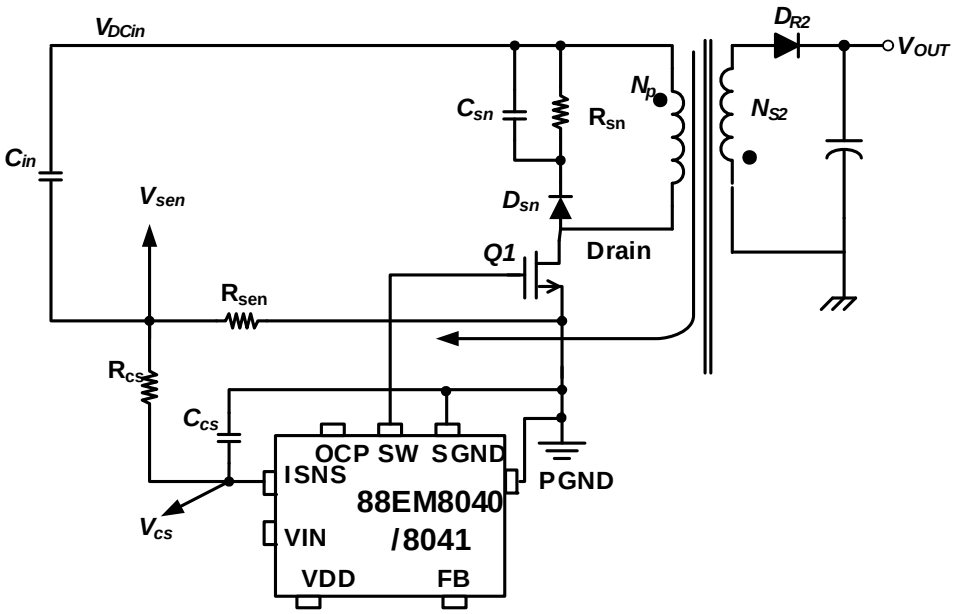


5.3 Current Sensing and Over Current Protection

5.3.1 Current Sensing Through ISNS Pin

The voltage drop on the current sense resistor should be kept very small in order to reduce the power consumption on the sense resistor. In flyback topology, the drain to source current flows through the transformer, MOSFET and current sense resistor (R_{sen}). This is shown in Figure 23. The average current mode control single stage solution requires two signals of flyback: the peak current signal to avoid the transformer saturation including a short circuit condition, and the average current sense signal to achieve the right PFC operation. The voltage drop (V_{sen}) across resistor (R_{sen}) represents the flyback peak current signal. The voltage of (V_{CS}), after R_{CS} and C_{CS} low pass filter, represents the average current signal of the primary side of the flyback converter.

Figure 23: Current Sensing Circuit



The resistor (R_{sen}) should be designed such as the example in Table 7 where R_{sen} is designed for a 90W adaptor. The specification are: output power = 90W, input voltage range = 85-264V, output voltage = 20V, output current= 4.5A, 30% margin of over current on top of the normal current.

Table 7: Current Sensing Circuit

Input Power	P_{in}	90W
Minimum input voltage	V_{inmin}	85V
Maximum average input current	$I_{inmax} = \sqrt{2} \times \frac{P_{in}}{V_{inmin}}$	1.49A
Over current threshold Zone 1	$V_{IOVERTH1}$	0.391V
Over current margin	I_{margin}	30%
Current sensing resistor calculation	$R_{sns} = \frac{V_{IOVERTH1}}{i_{inmax} \times (1 + I_{margin})}$	0.2Ω
Current sensing resistor selection	R_{sns}	0.2Ω

Table 8 shows the reference value of the current sensing resistor. In the practical design, the current sensing resistor value could be fine tuned around the value shown in the table based on the specification and the primary inductance of the flyback transformer.

Table 8: Current Sensing Resistor Selection Reference

Input Power (W)	36	72	90	120
Current Sensing Resistor (Ω)	0.40 - 0.45	0.20 - 0.27	0.15 - 0.20	0.12 - 0.15

5.3.2 Average Current Signal and Over Power Limitation

To convert flyback peak current into an average current signal, an RC filter is required. Figure 24 shows how adding two more components will result in an average current signal. This average current signal, V_{CS} is fedback onto the ISNS pin and used to achieve a sinusoidal current waveform by an internal current control loop. It is also used to achieve power limitation. The corner frequency of the RC filter is recommended approximately 1/10~1/6 of the switching frequency. R_{cs} is recommended as the value of 187Ω for the purpose of blocking negative and surge voltages. A single stage PFC operates at 120kHz (typical), C_{cs} is designed as 47nF which results in a corner frequency of 18kHz. The internal IC block is designed to perform the over power limitation as shown in the electrical characteristics table. The corner frequency of the low pass filter is designed as;

$$f_{corner} = \frac{1}{2\pi R_{cs} C_{cs}}$$ Equation (11)

5.3.3 Cycle by Cycle Current Protection through OCP Pin

In order to get the cycle by cycle current protection to avoid the transformer saturation, a circuit with a low base to emitter parasitic capacitance NPN transistor is recommended in the design, as shown in Figure 24. The sensing voltage through R_{sen} should trigger and turn on the transistor of Q2 during the over current condition. Q2 then pulls the OCP pin to low and turns off the gate signal to the external MOSFET. In order to get proper protection, a -2mV/°C (typical) temperature coefficient of (V_{be}) should be considered. The lowest voltage (V_{be}) will be set to the junction temperature of 80°C.

Figure 24: Current Sensing and Cycle by Cycle Over Current Protection Circuit

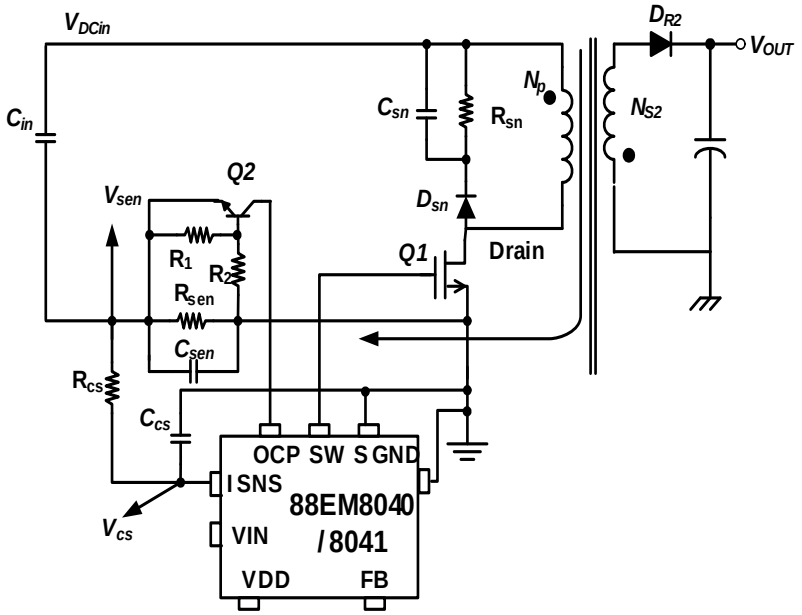
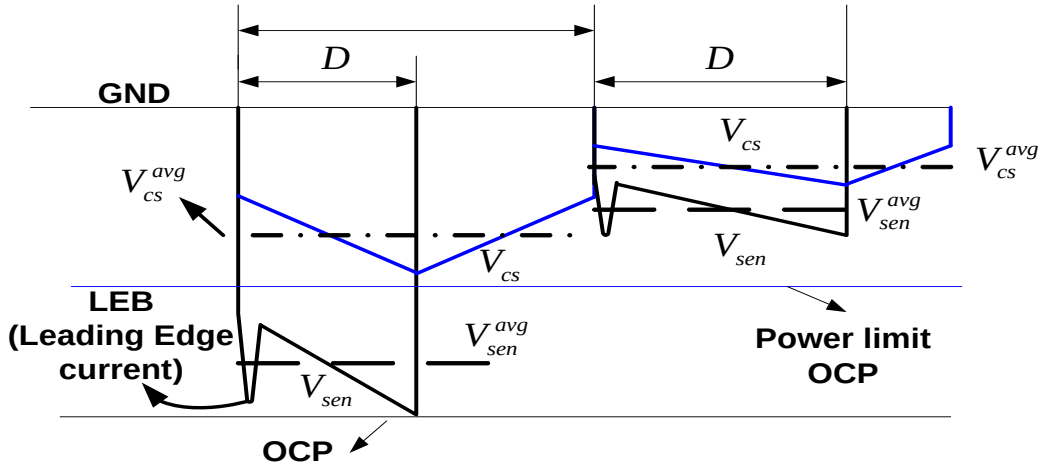


Figure 25: Current Sensing and Cycle by Cycle Over Current Protection Waveforms



$$V_{be} \cong 0.65V - 2mV \times (80 - 25) = 0.54V$$ Equation (12)

The highest V_{be} voltage will be set to the junction temperature of -25°C.

$$V_{be} \cong 0.65V - 2mV \times (-25 - 25) = 0.75V$$ Equation (13)

The voltage V_{be} is supposed to have some tolerance margin to select the resistor of R_{sen} without any unpredicted cycle by cycle over current protection. The recommended equation is:

$$R_{sen} \le \frac{0.50V}{I_{ds}^{peak}}$$ Equation (14)

The minimum saturation current point of I_{lim} for the transformer should satisfy:

$$I_{lim} = \frac{0.75V}{R_{sen}}$$ Equation (15)

I_{lim} should have enough margins considering transformer saturation condition at lower ambient temperature.

R_1 and R_2 should be selected properly in Figure 24, in order to make the cycle by cycle current limiting work correctly. R_1 and R_2 act as voltage dividers to setup the right current limitation threshold. Actually R_2 also works as controlling base current of that transistor, the same time, R_1 works to discharge the parasitic capacitance of that transistor. In the practical design, the R_1 and R_2 need to choose properly based on the power rating of the system. The value of R_1 is recommended as 500~2KΩ and R_2 as 500~2kΩ.

Please note that a small value of the capacitor parallel with the R_{sns} resistor is very helpful to filter the noise in order to guarantee this OCP circuit to function properly. When the MOSFET turns on, external C_{OSS} of the MOSFET starts discharging. This causes switching loss increases and makes the leading edge current. Figure 25 shows that this current creates unwanted over current making the system not function properly. This phenomenon can be avoided by adding one capacitor C_{sen}. The leading edge current timing is less than 300nS (typical). C_{sen} can be calculated as;

$$f_{sen} = \frac{1}{2\pi R_{sen} C_{sen}} \approx 1MHz$$ Equation (16)

C_{sen} is recommended to have a value of 0.22μF/25V.

5.3.4 Peak Current and Average Current Relationship

The relationship between the flyback peak and the average current signals are described in the following equation. Figure 25 explains this in detail.

Current sensing signal across Rsen resistor is calculated as

$$V_{sen} = R_{sen} \times I_{ds}$$ Equation (17)

The average current sensing signal during MOSFET switching on is

$$V_{sen}^{avg} = V_{sen} - R_{sen}\frac{\Delta I_{ins}}{2}$$ Equation (18)

The switching frequency peak to peak ripple is

$$\Delta I_{ins} = \frac{V_{line} \cdot D}{L_m \cdot f_s}$$ Equation (19)

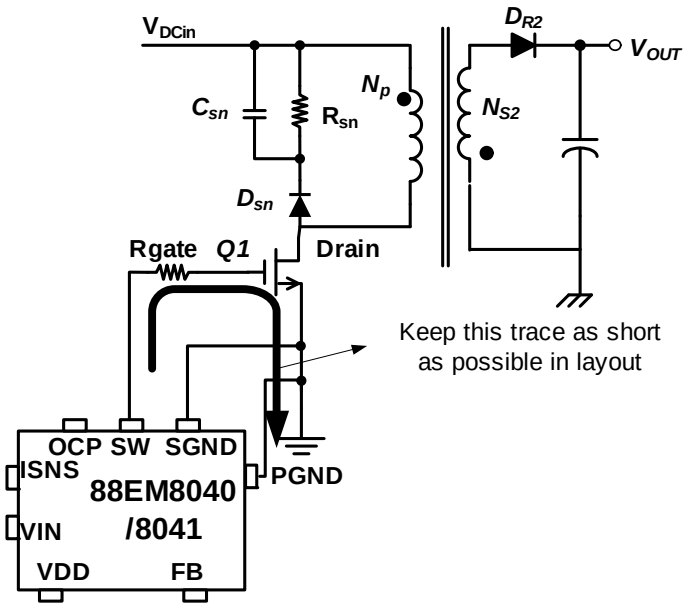
The average current sensing signal during the whole switching cycle is

$$V_{cs}^{avg} = V_{sen}^{avg} \times D$$ Equation (20)

5.4 SW Pin to MOSFET Gate

The 88EM8040/88EM8041 provides a maximum 2A drive current, which is the strongest driver capability in comparison with the other similar part on the market. A default resistor of 10Ω is designed to go between the SW pin and the gate of the external MOSFET. The gate driver loop is subject to fast rise and the layout trace should be kept as short as possible in order to minimize the parasitic inductance, as shown in Figure 26.

Figure 26: SW Pin Layout Guidelines



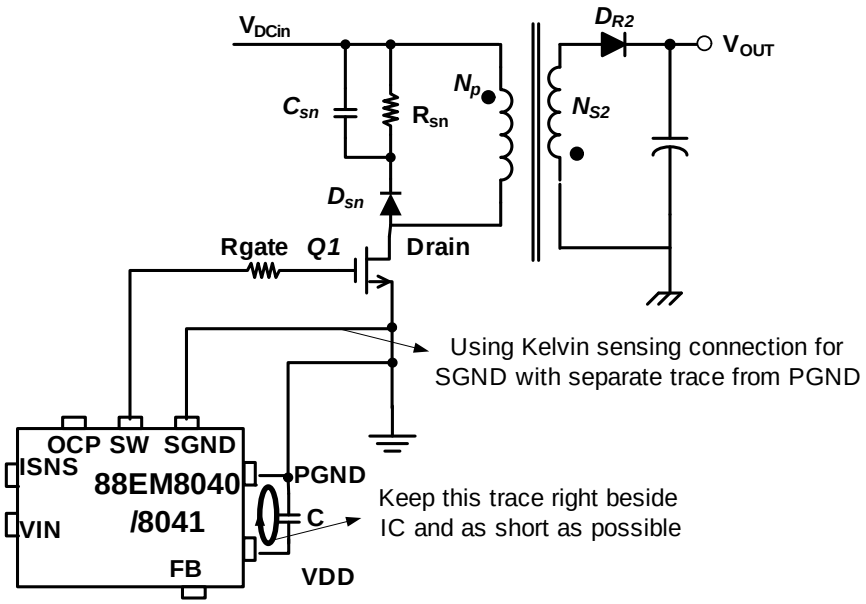
5.5 VDD, Signal Ground (SGND) and Power Ground (PGND)

VDD is the IC power supply pin. It has a typical input voltage value of 12V and a maximum operating voltage of 16V. A Zener clamp circuit of 16V is recommended in order to guarantee that the voltage on VDD will not go any higher than 16V. The IC begins to function when VDD powers on at 12V. Once the IC powers on, it keeps functioning as long as the VDD is higher than V_{DD_UVLO}, which is 7V (typical). In a practical design, an electrolytic capacitor 220μF (typical) is recommended to connect between VDD and ground in order to retain the IC functionality during startup. That capacitor will need to keep the VDD higher than 7V before the bias transformer winding takes over and provides enough energy for the power IC.

A 0.01-0.1μF ceramic capacitor is strongly recommended to be placed between the VDD and IC ground with the layout trace as close to the IC as possible. This capacitor is used for decoupling the noise to VDD and clamping the VDD voltage during the switching of the internal driver circuit.

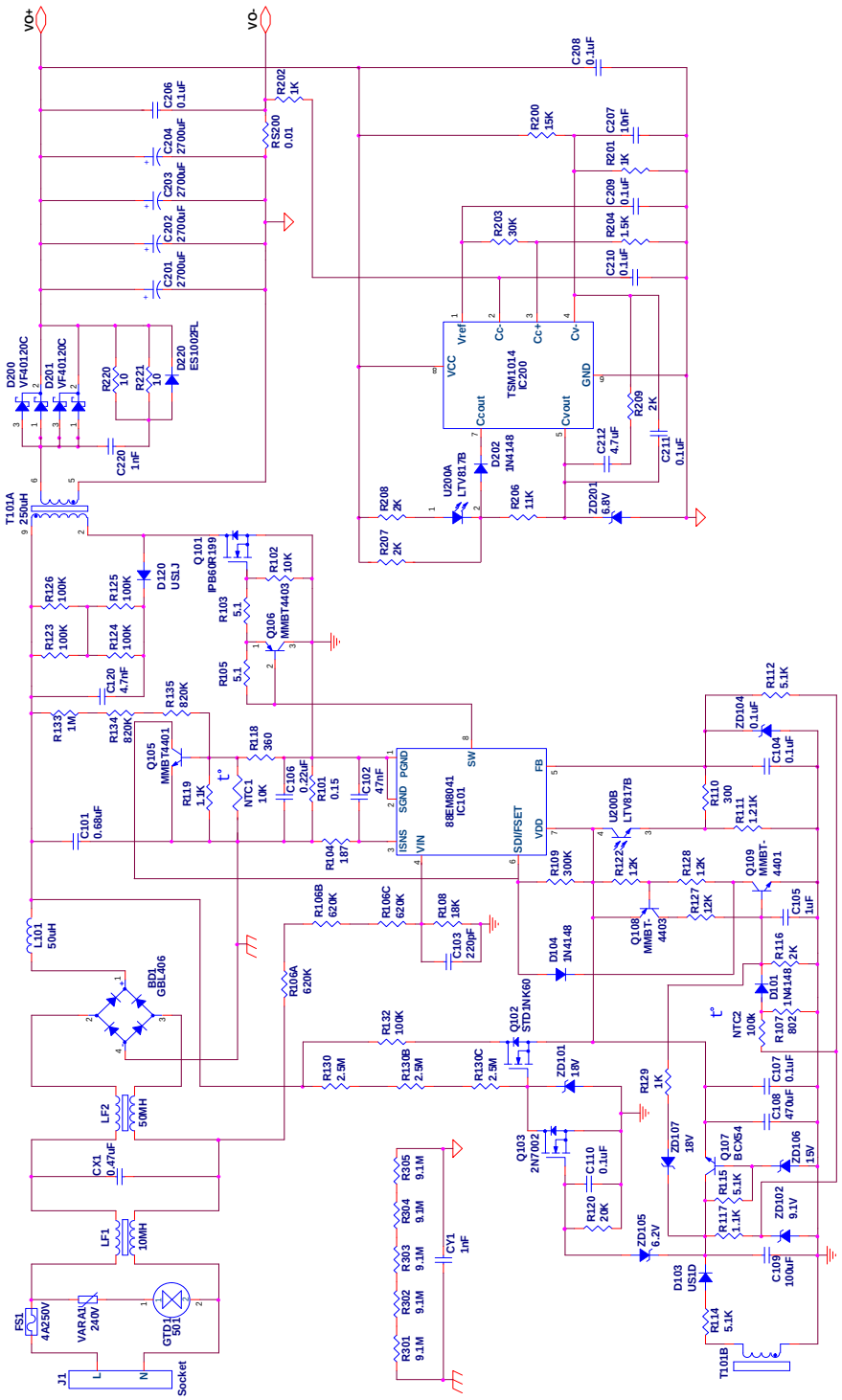
SGND is directly connected to the system ground by a Kelvin connection trace. The system ground is the source of the MOSFET, as shown in Figure 27. PGND connects to the system ground separately and can not share the same trace with SGND. This is due to pulse current on PGND while driving the external MOSFET on and off. This pulse current produces pulse voltage drops on the PGND trace and may cause the current sensing signal to be distorted if the SGND shares the same trace.

Figure 27: VDD Decoupling Capacitor and Ground Layout Guidelines



5.6 90W/20V Signal Stage PFC Adaptor Schematic and Bill of Materials (BOM)

Figure 28: 90W/20V Single Stage PFC Adaptor Schematic



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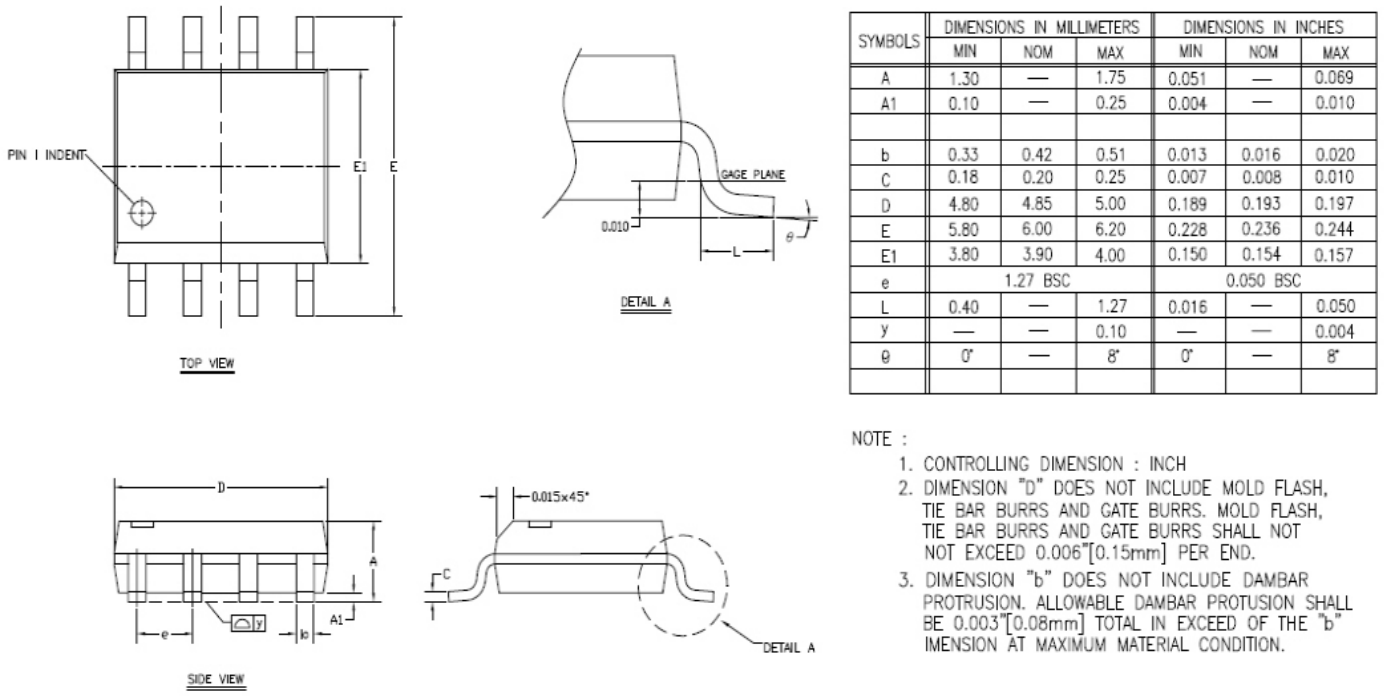
6.1 Mechanical Drawings

Figure 29: 8-Lead SOIC Mechanical Drawing



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.30	—	1.75	0.051	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	0.42	0.51	0.013	0.016	0.020
C	0.18	0.20	0.25	0.007	0.008	0.010
D	4.80	4.85	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
L	0.40	—	1.27	0.016	—	0.050
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

NOTE :
1. CONTROLLING DIMENSION : INCH
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT NOT EXCEED 0.006"[0.15mm] PER END.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCEED OF THE "b" IMENSION AT MAXIMUM MATERIAL CONDITION.

Notes:

- All dimensions in mm.
- See Section 7, Part Order Numbering/Package Marking, on page 45 for package marking and pin 1 location.

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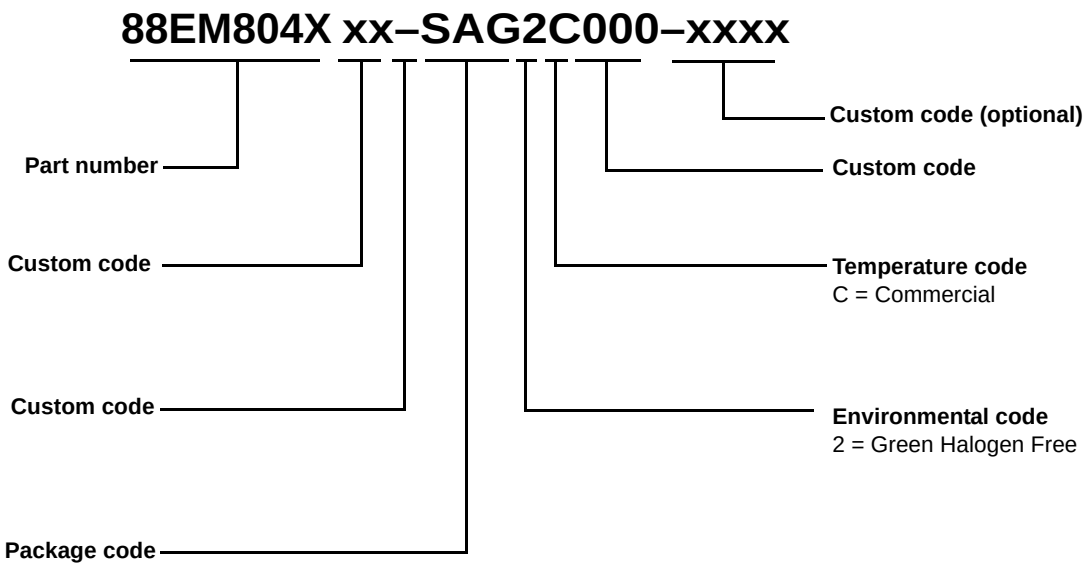
7 Part Order Numbering/Package Marking

7.1 Part Order Numbering

Figure 30 shows the part order numbering scheme. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 30: 88EM8040/88EM8041 Sample Ordering Part Number



The standard ordering part number for the respective solution is shown in Table 9.

Table 9: 88EM8040/88EM8041 Part Order Options[1]

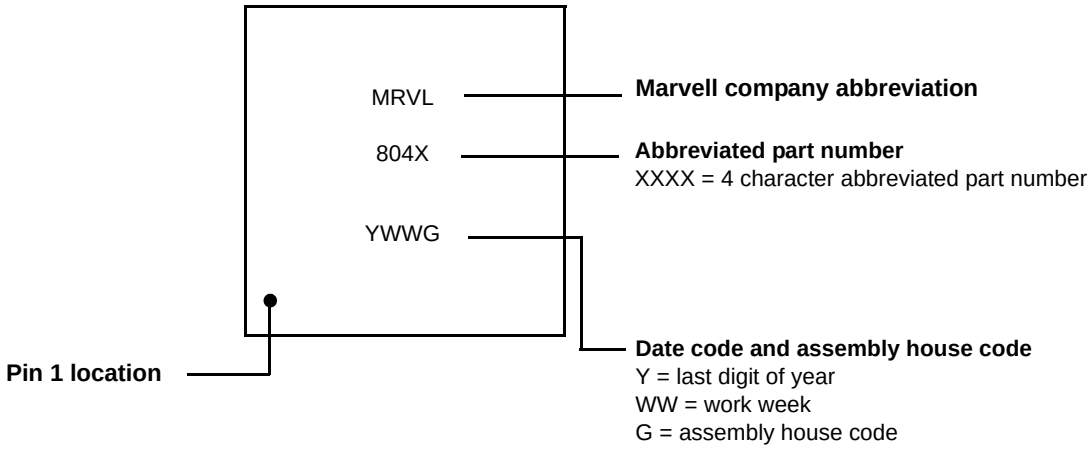
Package Type	Part Order Number
8-Pin SOIC	88EM8040xx-SAG2C000
8-Pin SOIC	88EM8040xx-SAG2C000-T (Tape and Reel)
8-Pin SOIC	88EM8041xx-SAG2C000
8-Pin SOIC	88EM8041xx-SAG2C000-T (Tape and Reel)

1. Please note that the 88EM8040 device is 60kHz and the 88EM8041 device is 120kHz.

7.2 Package Markings

Figure 31 shows a typical package marking and pin 1 location.

Figure 31: 88EM8040/88EM8041 Package Marking



Note: The above example is not drawn to scale. Location of markings are approximate.

A Revision History

Table 10: Revision History

Document Type	Document Revision
Release	8040/41 Rev. A
• Revised EC table with new values. • Reworked Application and Design Section • Revised Mechanical Drawing • Updated Part Ordering	
Release	8041 Rev. –
First Release	

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